an input circuit coupled to the input/output pin, wherein the input circuit, when active, transfers the input signal received from the input/output pin to the sound processing circuit; and

a control circuit coupled to the sound processing circuit, wherein the control circuit selects an operation performed by the processing circuit when the activation circuit activates the sound processing circuit, and

wherein the sound processing circuit comprises:

a first functional unit that performs an output operation to generate a signal to the output circuit and a second functional unit that performs an input operation to processes the input signal from the input circuit;

a memory array;

a read circuit coupled to the memory array, wherein the read circuit is part of the first functional unit and the output operation includes reading from the memory array a series of values representing a sound; and

a write circuit coupled to the memory array, wherein the write circuit is part of the second functional unit and the input operation includes writing to the memory array a series of values representing the input signal.

18.(Twice Amended) The integrated circuit of claim 17, wherein the activation circuit comprises a delay element coupled to prevent the activation circuit from activating the sound processing circuit during a delay period following completion of an operation by the sound processing circuit.

19.(Amended) The integrated circuit of claim 17, further comprising a die and a three-pin package in which the die is mounted, the three-pin package having exactly three pins including the input/output, a pin for connection to a power supply, and a pin for connection to ground.--

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REMARKS

These remarks are in response to the Office Action mailed April 11, 2001, setting a response period expiring on July 11, 2001, and for which a one-month extension is hereby requested. In that Office Action, all of the pending claims, claims 2, 4-9, and 11-36,